



TRANSMITTAL LETTER
(General - Patent Pending)

Docket No.
51889/2

In Re: Application Of: Douglas R. Hackler, Sr. et al.

Serial No.
10/613,169

Filing Date
July 3, 2003

Examiner
Not yet assigned

Group Art Unit
2811

Title: MULTI-CONFIGURABLE INDEPENDENTLY MULTI-GATED MOSFET

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Information Disclosure Statement
PTO-1449 with copies of cited references
Postcard

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of _____ is attached.
- ☐ The Director is hereby authorized to charge and credit Deposit Account No. _____ as described below.
- ☐ Charge the amount of _____
- ☐ Credit any overpayment.
- ☐ Charge any additional fee required.

Signature

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Dated: October 31, 2003

I certify that this document and fee is being deposited on Oct. 31, 2003 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

John R. Thompson

Typed or Printed Name of Person Mailing Correspondence

CC:



PATENT APPLICATION
Docket No.: 51889/2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)	
)	
Douglas R. Hackler, Sr. et al.)	
)	Art Unit
Serial No.: 10/613,169)	2811
)	
Filed: July 3, 2003)	
)	
For: MULTI-CONFIGURABLE INDEPENDENTLY)	
MULTI-GATED MOSFET)	

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97

TO THE COMMISSIONER FOR PATENTS:

Pursuant to his (her) (their) duty of disclosure, applicant(s) enclose(s) copies (a copy) of the document(s) listed on the accompanying Form PTO-1449.


1. This information disclosure statement is being submitted:

- a. ☒ Within three months of the filing date of the above-identified application or within three months of the date of entry of the national stage, or before the mailing date of the first Office action on the merits, whichever event occurs last. (No statement under 37 CFR 1.97(e) is required.)
- b. ☐ After the period set forth in paragraph 1a, but before the mailing date of either a final action or a notice of allowance. (Check box i. or ii.)
 - i. ☐ A \$180.00 information disclosure statement submission fee set forth in 37 CFR 1.17(p) is enclosed.
 - ii. ☐ A statement specified by 37 CFR 1.97(e) is set forth below.

- c. ☐ After the mailing date of a final action or notice of allowance and on or before payment of an issue fee. A statement specified by 37 CFR 1.97(e) is set forth below. A petition requesting consideration of the information disclosure statement and the \$130.00 petition fee set forth in 37 CFR 1.17(i) are enclosed.
- d. ☐ Concurrent with the filing of a Request for Continued Examination
2. ☐ The attorney or agent signing below hereby states that:
- a. ☐ each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.
- b. ☐ no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement.
3. ☐ Applicant(s) set forth below concise explanations of the relevance of each document not in the English language and/or selected document(s) in the English language.

DATED this 31 day of October, 2003.

Respectfully submitted,


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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	1	2002/0187610 A1	12/12/02	Furukawa et al.	438	283	06/12/01
	2	2002/0153587 A1	10/24/02	Adkisson et al.	257	510	07/02/02
	3	2002/0140039 A1	10/03/02	Adkisson et al.	257	377	06/18/02
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	6	2003/0089930 A1	05/15/03	Zhao	257	256	11/07/02
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	16	5,436,506	07/25/95	Kim et al.	257	347	10/12/93

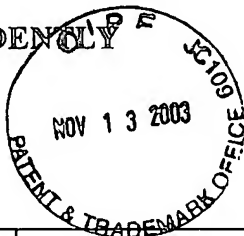
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	17	5,349,228	09/20/94	Neudeck et al.	257	365	12/07/93
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICA- TION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	20							
	21							
	22							
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OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication, etc.)

	28	Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004.
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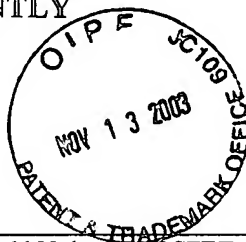
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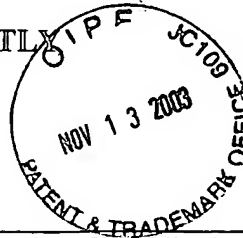
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48	Hisamoto, Digh, "FD/DG-SOI MOSFET – a viable approach to overcoming the device scaling limit," Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185-8601, Japan, pgs. 19.3.1-19.3.4.
49	Kedzierski et al., "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, 94720, USA, pgs. 3.4.1-3.4.4.
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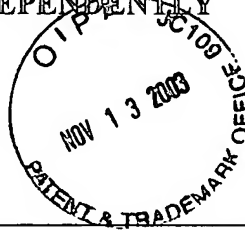
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62	Jeong et al., "High Performance Double-Gate Device Technology Challenges and Opportunities," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY, USA, pgs. 492-495.
63	Chang et al., "Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 31.2.1-31.2.4.
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65	Yagishita et al., "Dynamic Threshold Voltage Damascene Metal Gate MOSFET (DT-DMG-MOS) with Low Threshold Voltage, High Drive Current, and Uniform Electrical Characteristics," Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.2.1-29.2.4.
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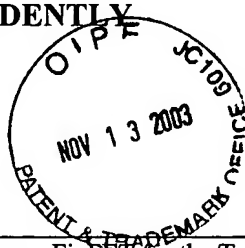
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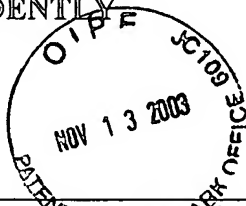
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